# M5M4V4169TP-15,-20

4MCDRAM:4M(256K-WORD BY 16-BIT) CACHED DRAM WITH 16K (1024-WORD BY 16-BIT) SRAM

*Preliminary*
**This document is a preliminary Target Spec. and some of the contents are subject to change without notice.**

## DESCRIPTION

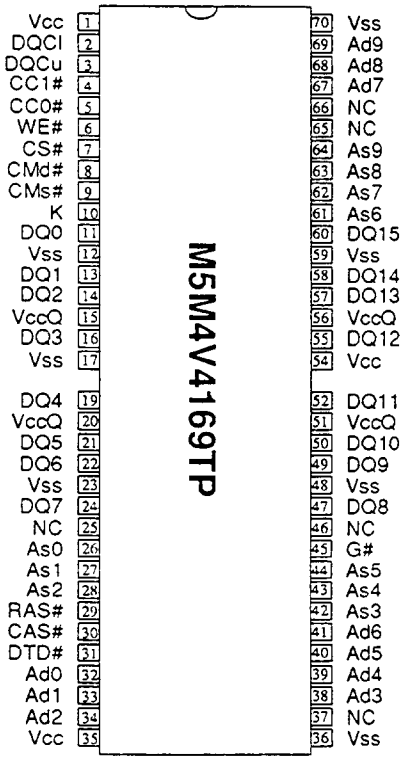
1. The M5M4V4169TP is a 4M-bit Cached DRAM which integrates input registers, a 262,144-word by 16-bit dynamic memory array and a 1024-word by 16-bit static RAM array as a Cache memory (block size 8x16) onto a single monolithic circuit. The block data transfer between the DRAM and the data transfer buffers (RB/WB1/WB2) is performed in one instruction cycle, a fundamental advantage over a conventional DRAM/SRAM cache.
2. The RAM is fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low cost are essential. The use of quadruple-layer polysilicon process combined with silicide and double layer aluminum wiring technology, a single-transistor dynamic storage stacked capacitor cell, and a six-transistor static storage cache cell provide high circuit density at reduced costs.

## FEATURES

| Type name | SRAM Access/cycle | DRAM Access/cycle | Power Dissipation (Typ) |
|---|---|---|---|
| **M5M4V4169TP-15** | 15ns/15ns | 75ns/120ns | DRAM: 220mW<br>SRAM: 580mW |
| **M5M4V4169TP-20** | 20ns/20ns | 80ns/140ns | DRAM: 200mW<br>SRAM: 470mW |

- 70-pin,400-mil TSOP (type II ) with 0.65mm lead pitch and 23.49mm package length.
- Multiplexed DRAM address inputs for reduced pin count and higher system densities.
- Selectable output operation (transparent / latched / registered) using set command register cycle.
- Single 3.3V +/- 0.3V Power Supply.
- 1024 refresh cycles every 16ms (Ad0->Ad9).
- Synchronous design for precise control with an external clock (K).
- Output retention by advanced mask clock (CMs#).
- All inputs/outputs low capacitance and LVTTL compatible.
- Asynchronous output enable (G#) for bus control.
- Separate DRAM and SRAM address inputs for fast SRAM access.
- Page Mode capability.
- Auto Refresh capability.
- Self Refresh capability.

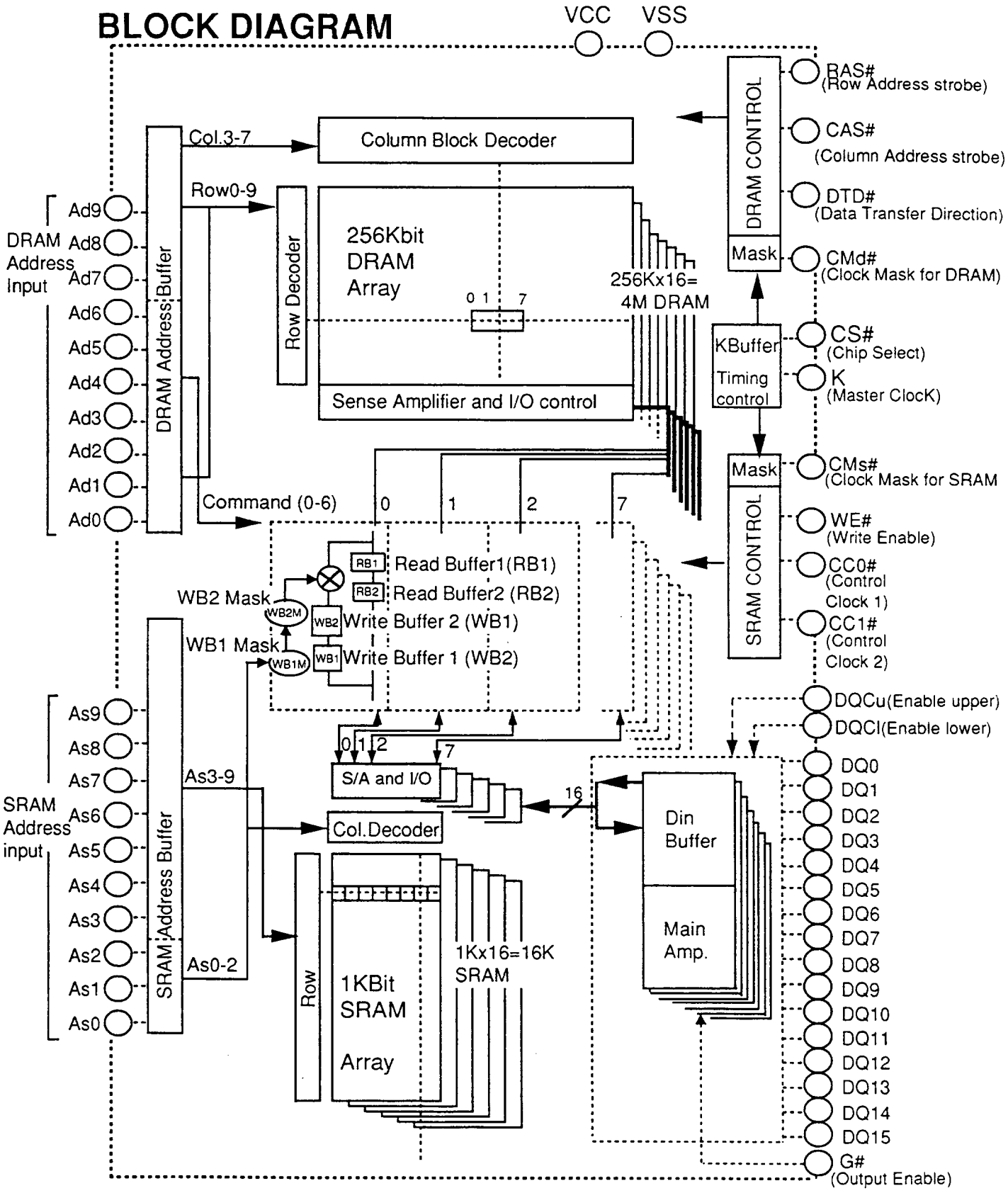
## PIN CONFIGURATION (TOP VIEW)



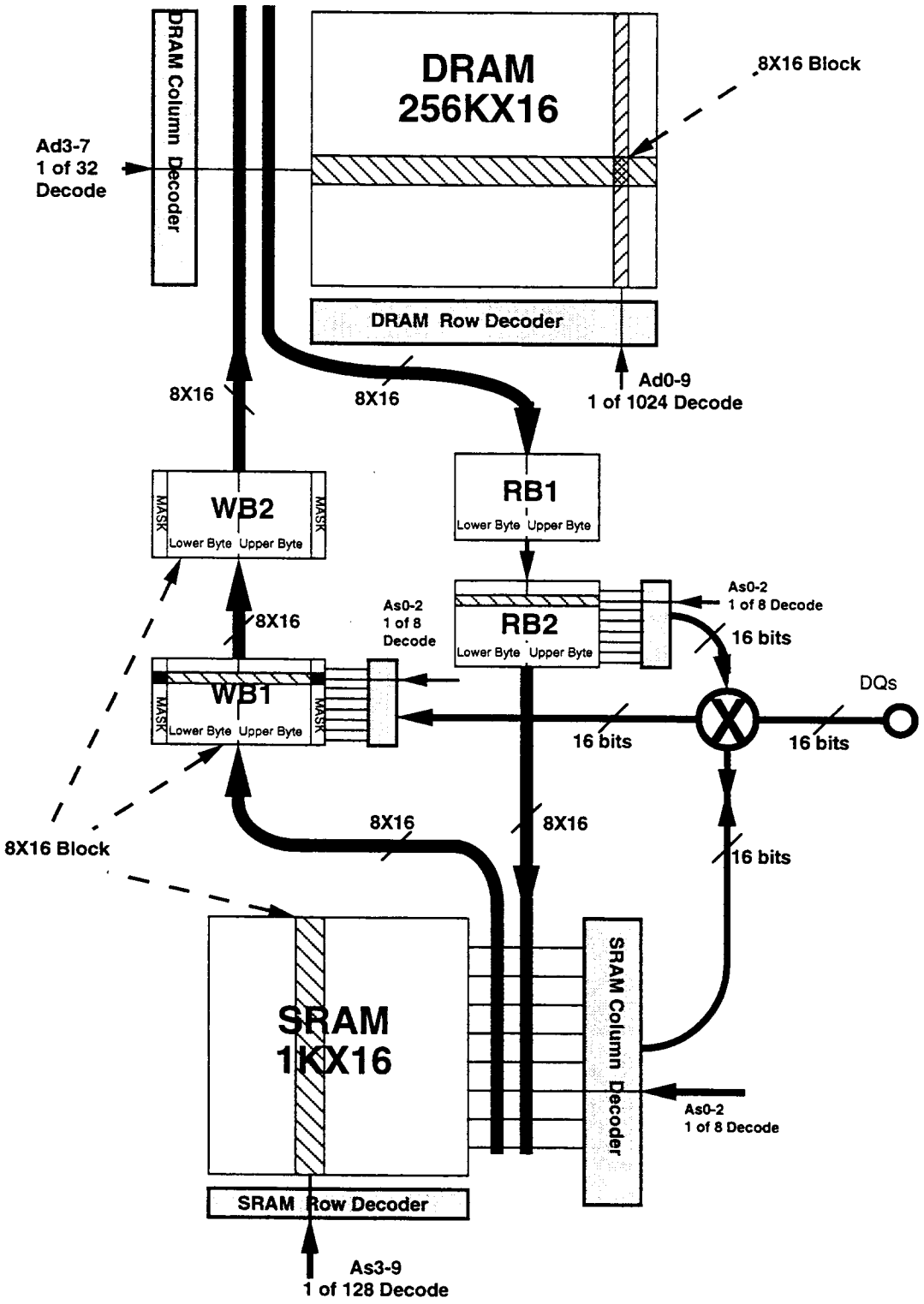

Package code:70P3S-L

| | |
|---|---|
| K | : Master Clock |
| CS# | : Chip Select |
| CMd# | : DRAM Clock Mask |
| RAS# | : Row Addr. Strobe |
| CAS# | : Column Addr. Strobe |
| DTD# | : Data Transfer Direction |
| Ad | : DRAM Address |
| CMs# | : SRAM Clock Mask |
| CC0#,CC1# | : Control Clocks |
| WE# | : SRAM Write Enable |
| DQC(u/l) | : I/O Byte Control |
| As | : SRAM Address |
| G# | : Output Enable |
| DQ | : Data I/O |
| Vcc | : Power Supply |
| VccQ | : DQ Power Supply |
| Vss | : Ground |

# BLOCK DIAGRAM

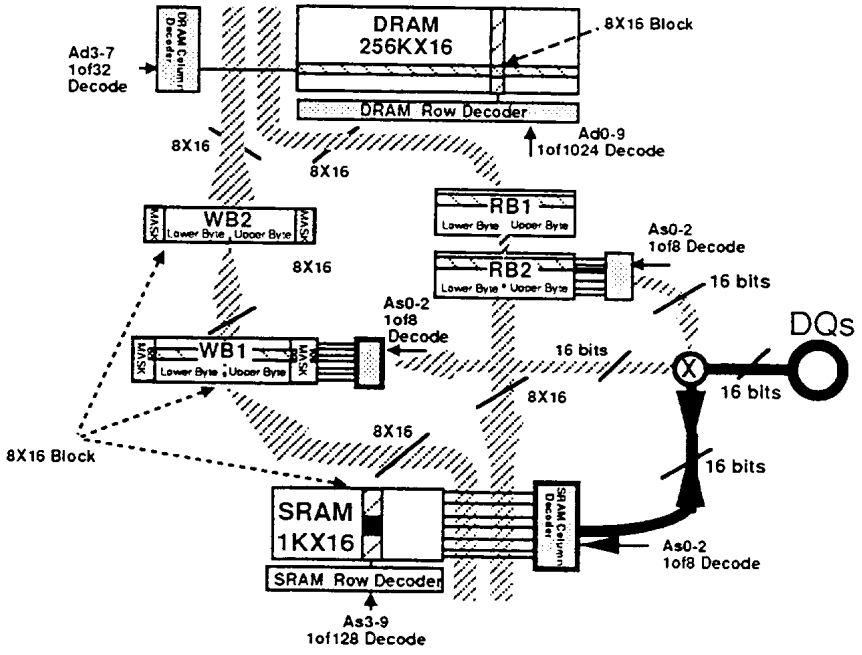


## BLOCK DIAGRAM #2

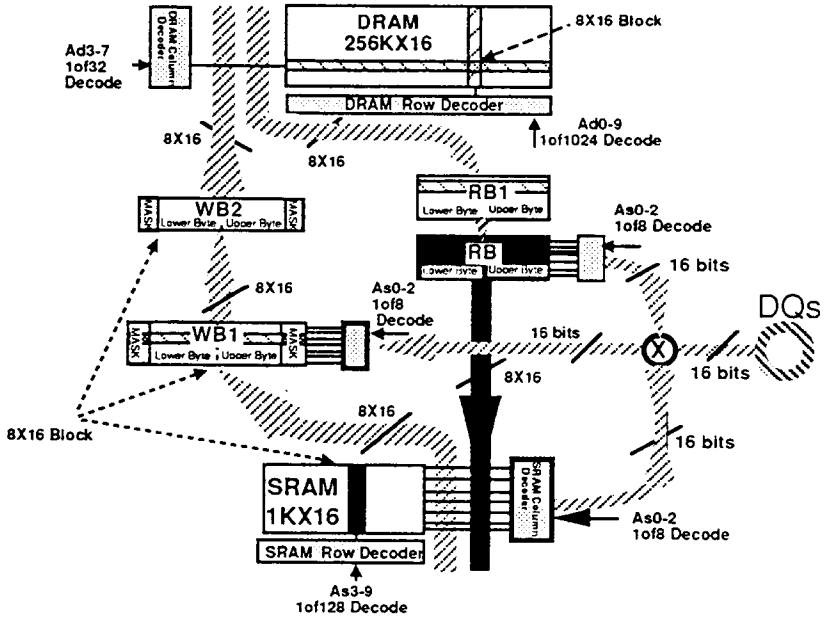
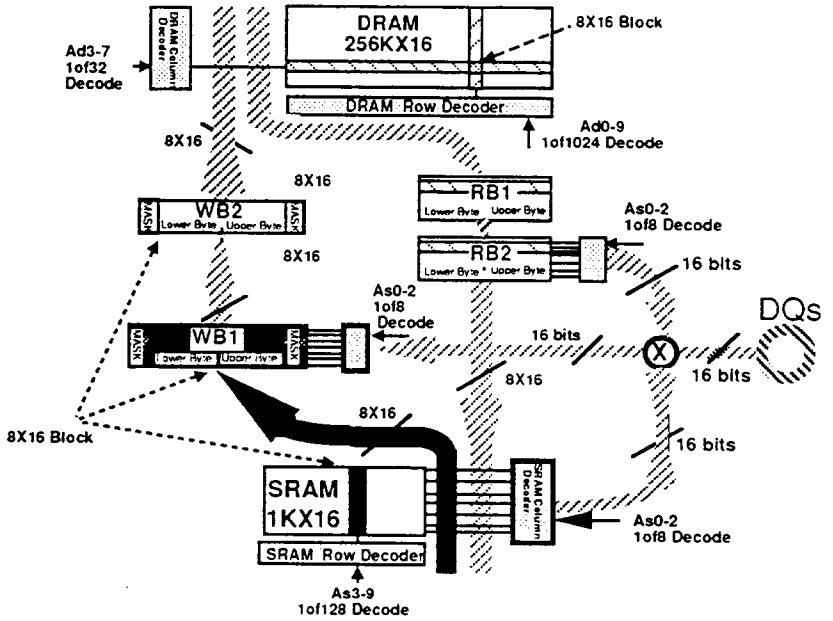


# MODE DESCRIPTIONS (1)

| | |
|---|---|
| NOP | No Operation. Outputs are high-impedance. All input buffers remain active. |
| SRAM Power-Down | If CMs#=Low at the rising edge of K, the SRAM enters SRAM Power Down at the next rising edge of K. During this mode, the internal SRAM K clock becomes inactive. The Output Buffers remain enabled and are controlled by G#. All input buffers of SRAM clocks and SRAM addresses are inactive. |
| Deselect SRAM | All transfer functions and input/output operations to and from the SRAM and Buffer are disabled. This cycle is useful for output impedance control (Hi-Z,Low-Z) without G#. Internal output buffers are active during this cycle for registered output mode control. |
| SRAM Read | Data is read from the SRAM to the I/O pins. Addresses As0-As9 are used to select the data to be read. As3-As9 decode the SRAM Row (=Block), and As0-As2 decode (1 of 8) the 16-bit word. DQCu and DQCl control the impedence (High-Z/Low-Z) of the upper and lower bytes, respectively. |
| SRAM Write | Data is written from the I/O pins to the SRAM. Addresses As0-As9 are used to select the location to be written. As3-As9 decode the SRAM Row (=Block), and As0-As2 decode (1of8) the 16-bit word to be written. DQCU and DQCL control Upper and Lower byte writes, respectively. |



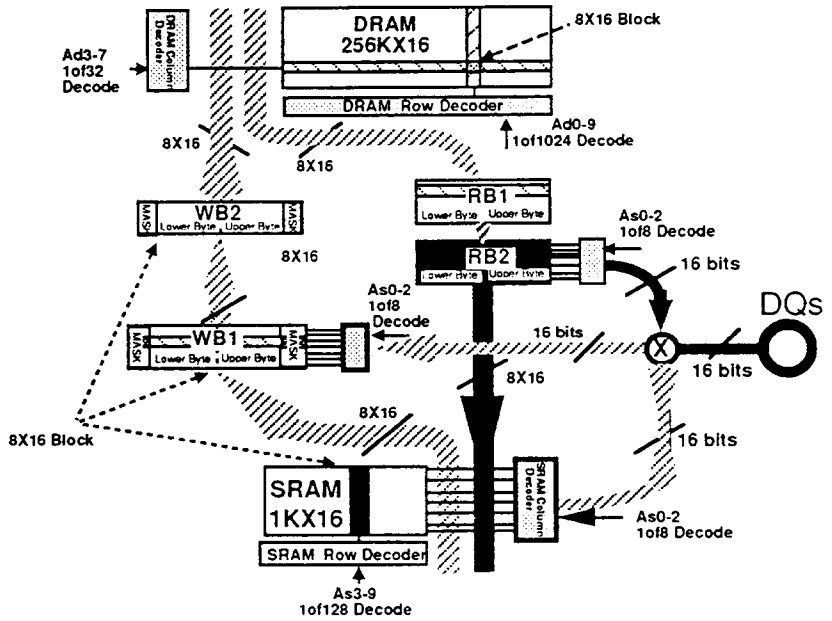
# MODE DESCRIPTIONS (2)

| | |
|---|---|
| Buffer Read Transfer | Data is transferred from the Read Buffer (RB) to the SRAM. Addresses As3-9 select the SRAM row to which the 8X16 bit block is to be written. Addresses As0-As2 must be set low.   |
| Buffer Write Transfer | Data is transferred from the SRAM to the Write-Buffer1 (WB1). Addresses As3-As9 decode the SRAM Row (=8X16 bit block) to be transferred. Addresses As0-As2 must be set low. The Buffer Write Transfer cycle "clears" all transfer mask bits in the WB1 Mask (allowing all data to be transferred in a successive DRAM Write Transfer cycle).   |

# MODE DESCRIPTIONS (3)

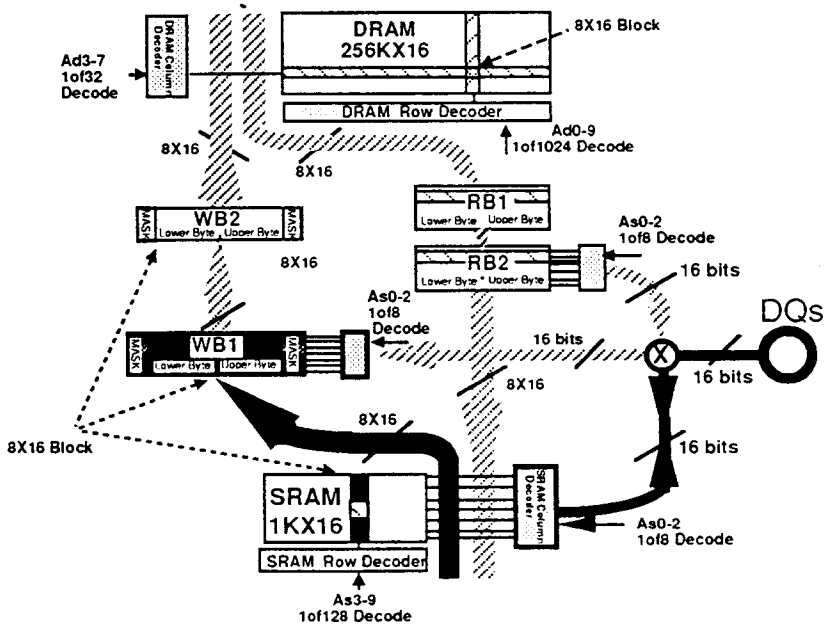
**Buffer Read Transfer & SRAM Read**

Data is transferred from the Read Buffer (RB) to the SRAM, and simultaneously, data (16 bit word) is read from the RB to the I/O pins. Addresses As3-9 select the SRAM Row to which the 8X16 bit block is to be written. Addresses As0-As2 decode the 16-bit word to be read.

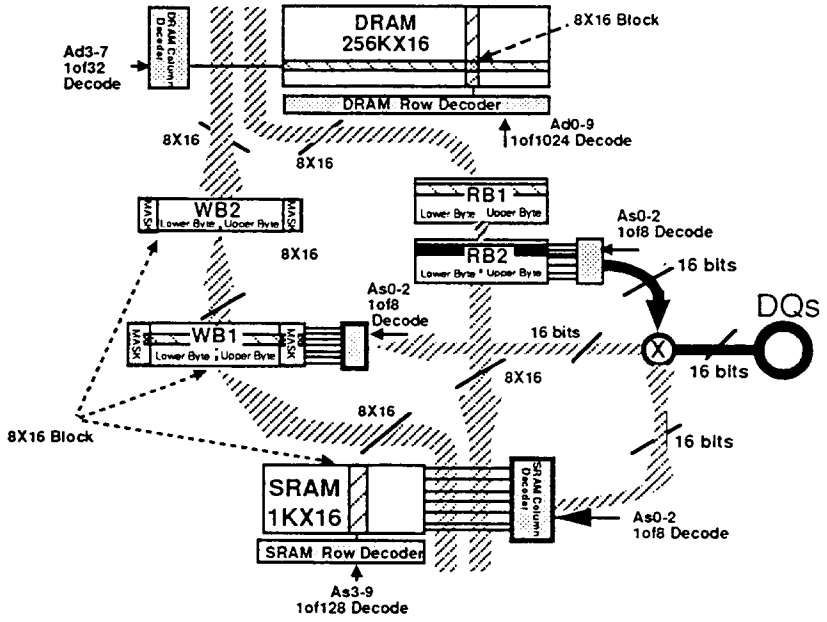
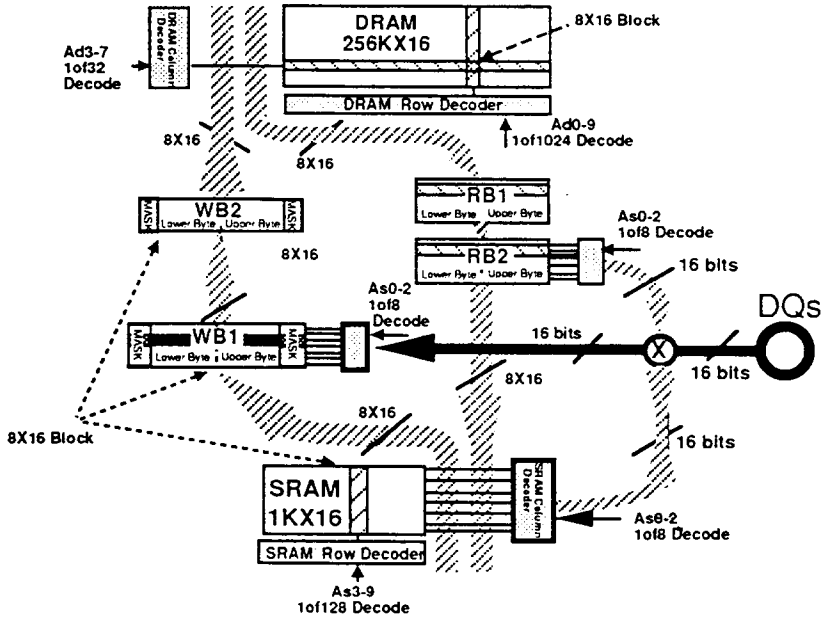



**Buffer Write Transfer & SRAM Write**

Data is first written from the I/O pins to SRAM as decoded by As0-As9. Then, the SRAM Row (=Block) decoded by As3-As9 is transferred to the Write-Buffer1 (WB1). The Buffer Write Transfer cycle "clears" all transfer mask bits in the WB1 Mask (allowing all data to be transferred in a successive DRAM Write Transfer cycle). DQCu and DQCl control upper and lower byte writes respectively, however all transfer mask bits in the WB1 are cleared.

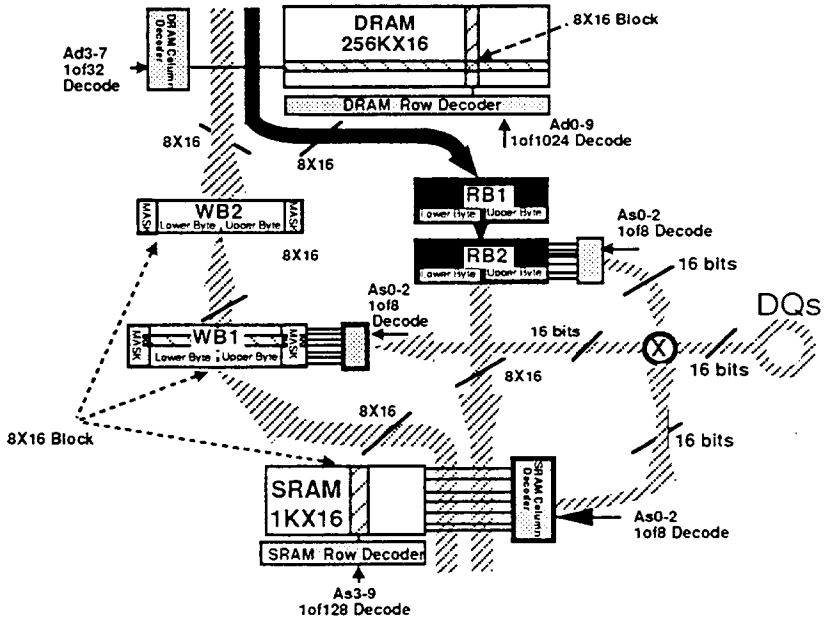


# MODE DESCRIPTIONS (4)

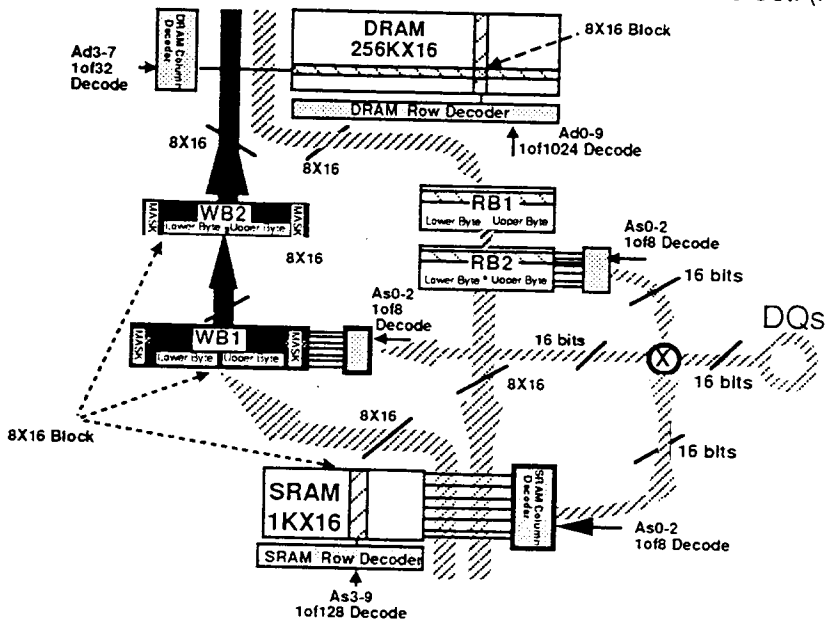
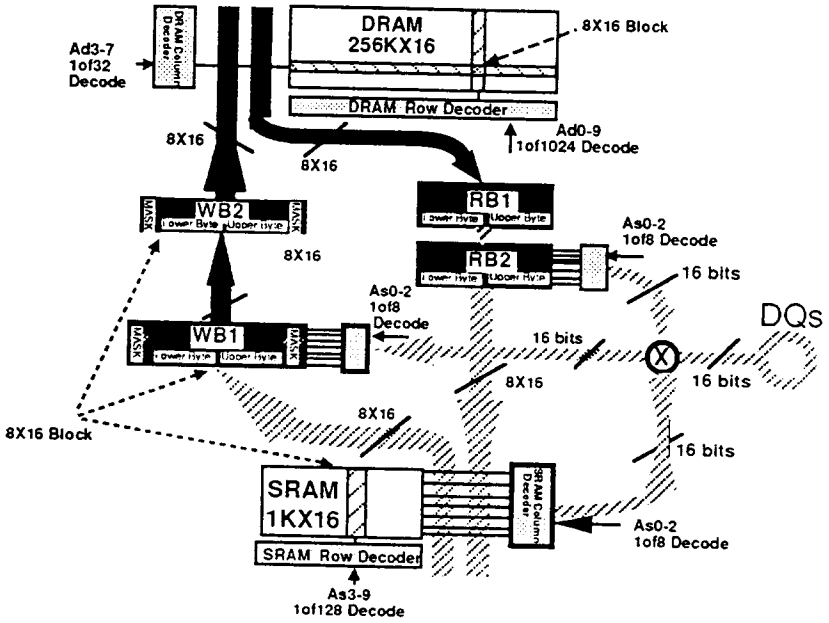
| | |
|---|---|
| Buffer Read | Data is read from the Read Buffer (RB) to the I/O pins. Addresses As0-As2 are used to select (1 of 8) the 16-bit word to be read. Addresses As3-As9 must be set low for this operation.   |
| Buffer Write | Data is written from the I/O pins to the Write-Buffer1. Addresses As0-A2 are used to select (1of8) the 16-bit word to be written. Addresses As3-As9 must be set low for this operation. The transfer mask bits associated with the Upper and Lower bytes are cleared in the WB1 Mask. DQCu and DQCl control Upper and Lower byte writes (and associated tranfer mask bits), respectively.   |

# MODE DESCRIPTIONS (5)

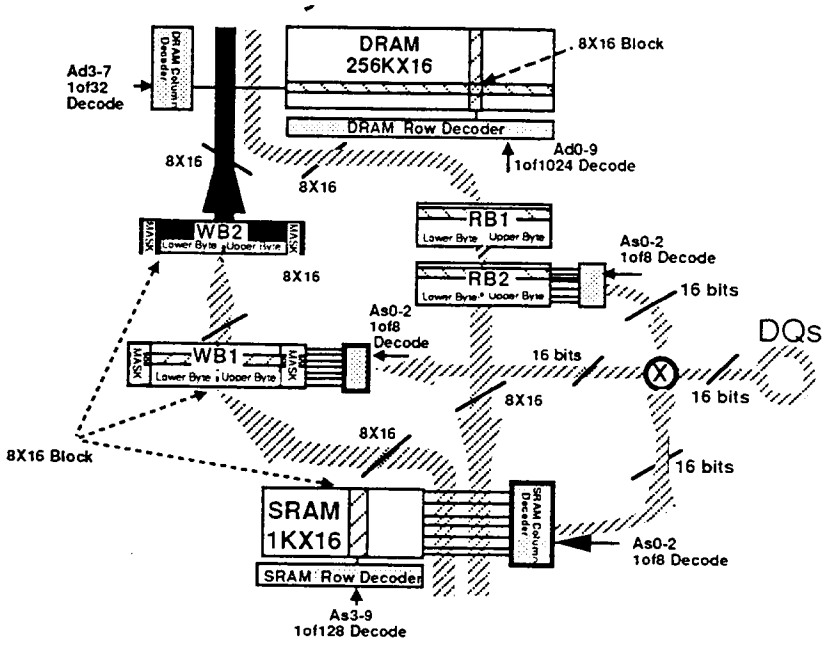
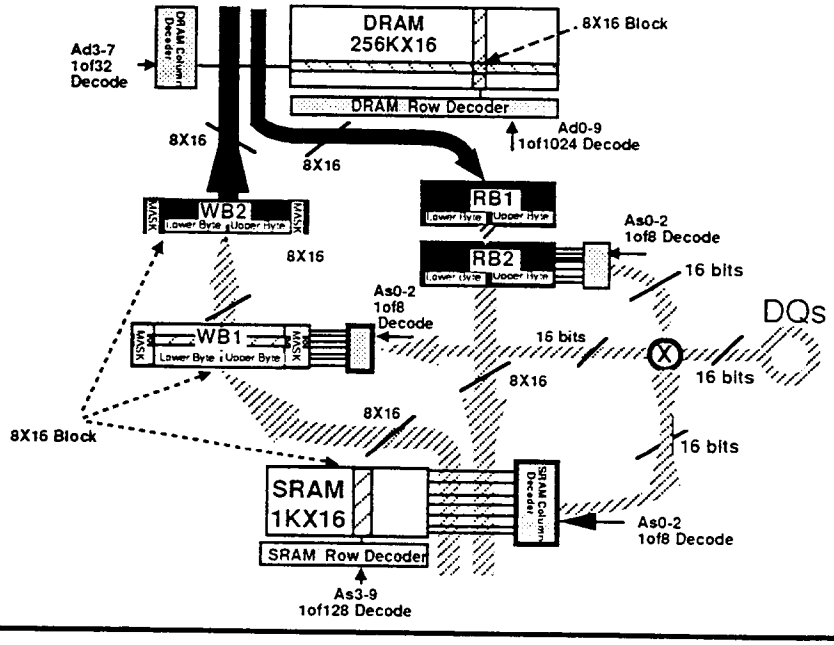
| | |
|---|---|
| DRAM Power-Down | If CMd#=Low at the rising edge of K, the DRAM enters DRAM Power Down at the next rising edge of K. During this mode, the internal DRAM K clock becomes inactive. Also all input buffers of DRAM clocks and DRAM addresses are inactive. Note that the latency of DRAM Read Transfer cycle is not counted up in this cycle. |
| DRAM NOP | The DNOP cycle is used when no other DRAM operations are desired, holding the DRAM in its present (precharge/activate) state. |
| DRAM Read Transfer | A Block (8X16) is transferred from the DRAM to the Read Buffer (RB) as specified by Addresses Ad3-Ad7. Addresses Ad8-Ad9 and Ad0-Ad2 must be set to Low. After the Latency Period (specified in the Access Latency Table) new data will be present in the Read Buffer. Prior to the Latency timeout, old data will be present in the RB. (Notes 1,2,4) |



# MODE DESCRIPTIONS (6)

| | |
|---|---|
| DRAM Write Transfer1 | Data (8X16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad9 must be set to Low. The Mask present in WB1 is also transferred to WB2 and controls the data written to the DRAM. After data has been transferred from WB1 to WB2 in the present cycle, the entire WB1 Mask is Set. (Notes 3,4)   |
| DRAM Write Transfer1 & Read | Data (8X16 Block) is transferred from WB1 through WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad9 must be set to Low. The transfer mask present in WB1 is also transferred to WB2 and controls the data written to the DRAM. The block to which the data is written in DRAM is simultaneously transferred to the Read Buffer.(Notes 2,3,4)   |

# MODE DESCRIPTIONS (7)

| | |
|---|---|
| DRAM Write Transfer2 | Data (8X16 Block) is transferred from WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad9 must be set to Low. The WB2 Mask controls the data written to the DRAM. With the DWT2 function, the WB2 data and WB2 Mask remain unchanged. (Note 4)   |
| DRAM Write Transfer2 & Read | Data (8X16 Block) is transferred from WB2 to the DRAM block specified by Addresses Ad3-Ad7. Addresses Ad8-Ad9 must be set to Low. The WB2 transfer mask controls the data written to the DRAM. With the DWT2 function, the WB2 data and WB2 transfer mask remain unchanged. The block to which the data is written in DRAM is simultaneously transferred to the Read Buffer. (Notes 1,2,4)   |